FINAL REPORT

UNIVERSAL VOICE PROCESSOR DEVELOPMENT

CONTRACT NAS9-11961

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REFERENCE DOCUMENTS

DOCUMENT	TITLE
MIL-STD-883	TEST METHODS & PROCEDURES FOR MICROELECTRONICS
MIL-M-38510	GENERAL SPECIFICATIONS FOR MICROCIRCUITS
SD 70-155-3-4	INFORMATION SUBSYSTEM, VOL. 3, PART 4, "SPACE STATION DEFINITION STUDY, PHASE B", CONTRACT NAS9-9953
NAVWEPS OD30355	STANDARD HARDWARE PROGRAM

FINAL REPORT

UNIVERSAL VOICE PROCESSOR DEVELOPMENT

This report will discuss all work performed by General Electric on contract No. NAS9-11961 beginning on 14 June 1971 through final completion. In initial meetings between GE and NASA personnel, a discussion of the use of hybrid circuit techniques in execution of the contract were reaffirmed as stated in Volume I, Technical Proposal for the Univeral Voice Processor Development, submitted in response to National Aeronautics and Space Administration, Manned Spacecraft Center, RFP No. BC73-50-1-157P. GE stated that by using hybrid techniques, several circuit configurations could possibly satisfy the electrical specifications so emphasis would be on optimizing the design for manufacturability. Once the design is firm, quick reaction will be afforded by the hybrid approach.

For the purposes of this report, the evolution of the circuit development will be presented to conform with the block diagram (Fig. 1) in the following order:

I AGC Circuit

II Input Amplifiers

a. High Level

b. Low Level

III Clipper

IV Voice Operated Switch (VOX)

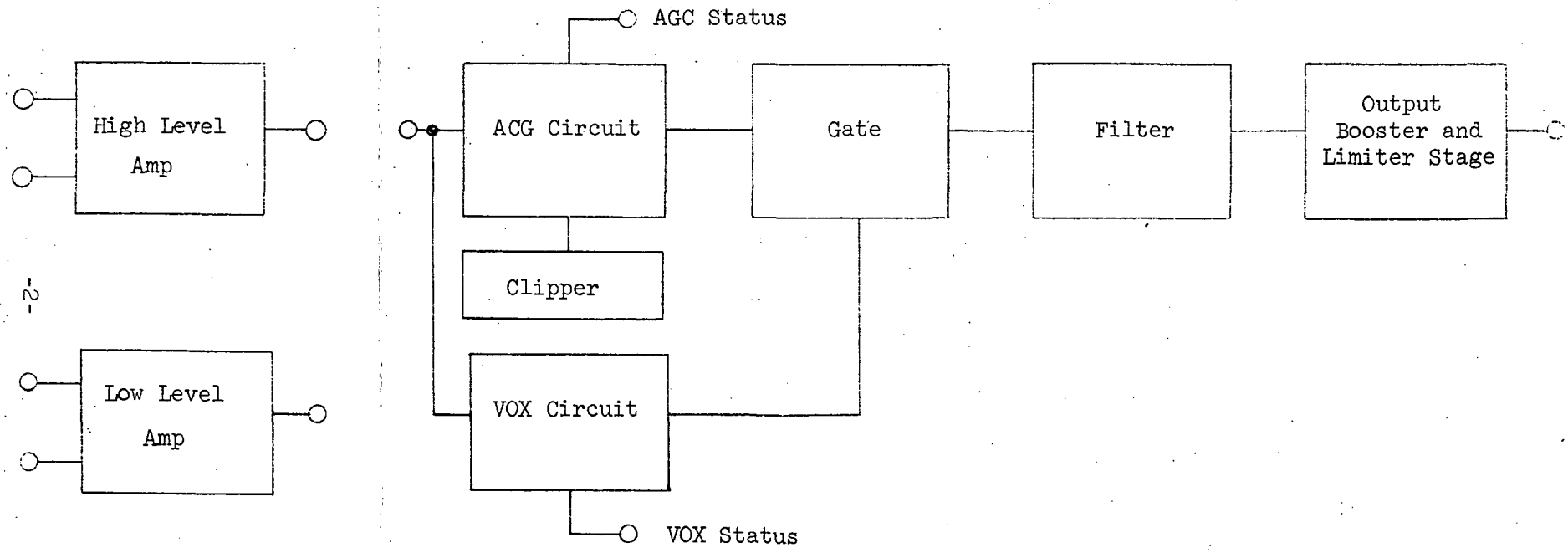
a. Level Sense

b. Gate

V Filter

VI Output Booster and Current Limiter Stage

VII Power Conditioning



UVP BLOCK DIAGRAM

FIGURE 1

I. AGC Circuit

Initial design was started with the use of an integrated circuit AGC amplifier being the principal control element of the design. Three different AGC circuits were breadboarded and tested using the LM370 (National Semiconductor) AGC amplifier. The circuits suggested by National Semiconductor and subsequent circuit designs by General Electric used large value capacitors (1 mfd). This was finally eliminated by the circuit shown in Figure 2. The design was reduced to a breadboard and did not require input amplifiers. The amplification for the low level input was provided in the AGC circuit, as well as the necessary differential to single-ended signal conversion. The high level input was then reduced, by resistive dividers, so that it could be processed by the same AGC circuit. This approach was considerably simpler than the design described in the Design Performance Specification Report, but failed to meet the performance requirements in three respects:

1) The exact input level at which the AGC could produce 0 dbm was not predictable as the exact value of open loop gain for the LM370 (used in the AGC) was not predictable.

2) The level at which VOX action initiated was not well controlled due to the necessity of using the AGC output as the VOX signal input.

3) The ability to generate an external indication of AGC status was doubtful due to the closed loop operation of the LM370 which resulted in small and unpredictable AGC control signals.

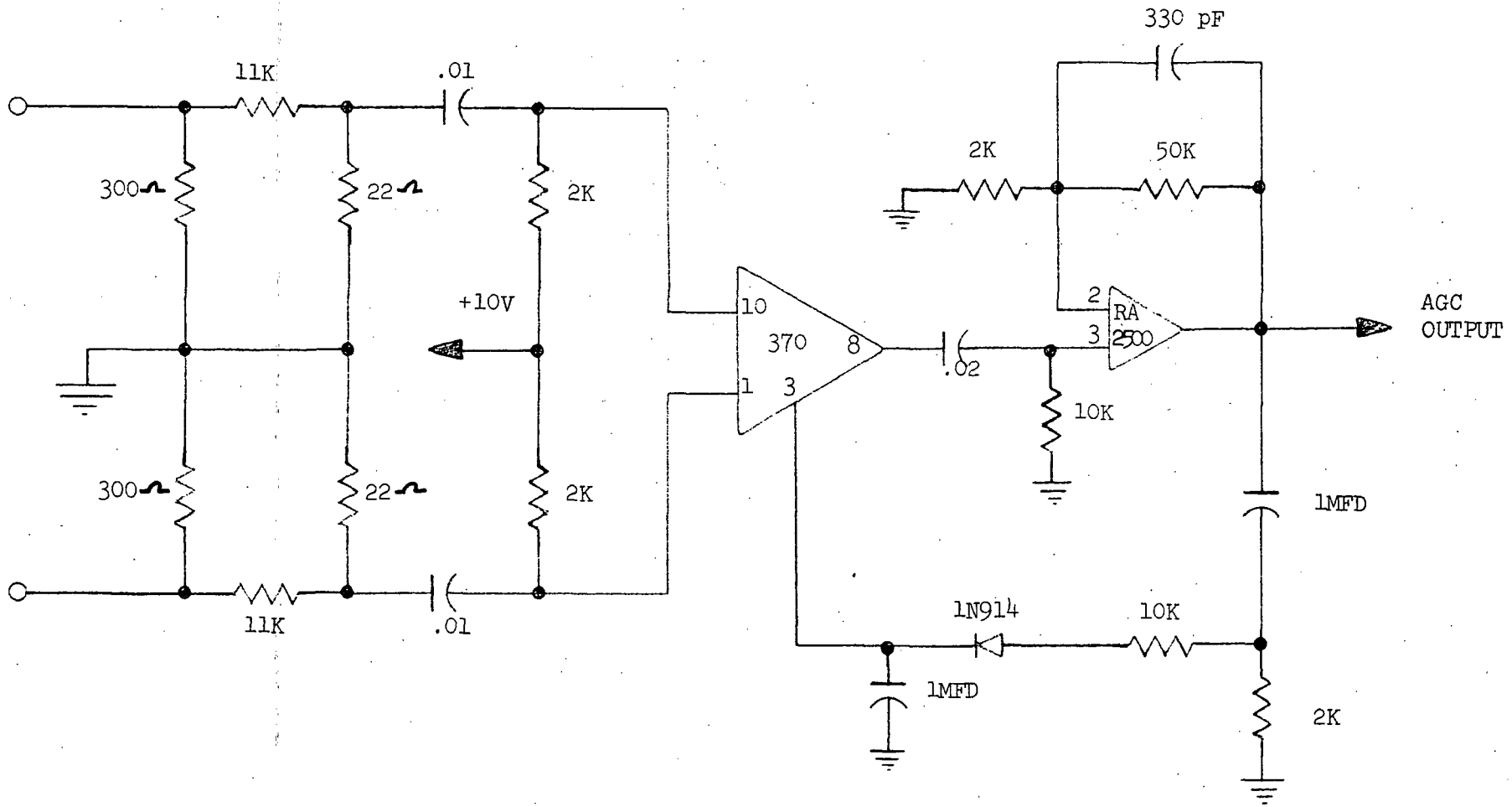

11K
.01
300
22
2K
+10V
300
22
2K
11K
.01
10
370
8
1
3
330 pF
2K
50K
2
RA
3
2500
AGC
OUTPUT
.02
10K
1MFD
1N914
10K
1MFD
2K

FIGURE 2

Additionally, the distortion exhibited by the LM370, while not excessive, was considerably greater than that produced in the final circuit. As a result of the above deficiencies the design was changed to a completely new circuit concept.

The final design (Fig. 3) is an AGC circuit with a maximum gain of 25db. Because of this, a gain of -25db is required from the high level input amplifier and a gain of +30db was required from the low level input amplifier. The signal range is normalized to the voltage equivalent of -25dbm to 0dbm on (for a sinusoidal signal) 123mv p-p to 2.19 volts p-p. The AGC provides a maximum gain of 25db (17.8 volts/volt) and a minimum gain of 0 db. This is accomplished by varying the effective resistance of Q1. The maximum gain is provided when Q1 is pinched off. The gain of the U1 stage of substrate A1 is then $-R4/(R2 + R3)$ or 17.8 volts/volt. Q1 must be capable of reducing the gain by appearing as a low resistance. The equivalent resistance (R_E) needed can be calculated for the following relationships:

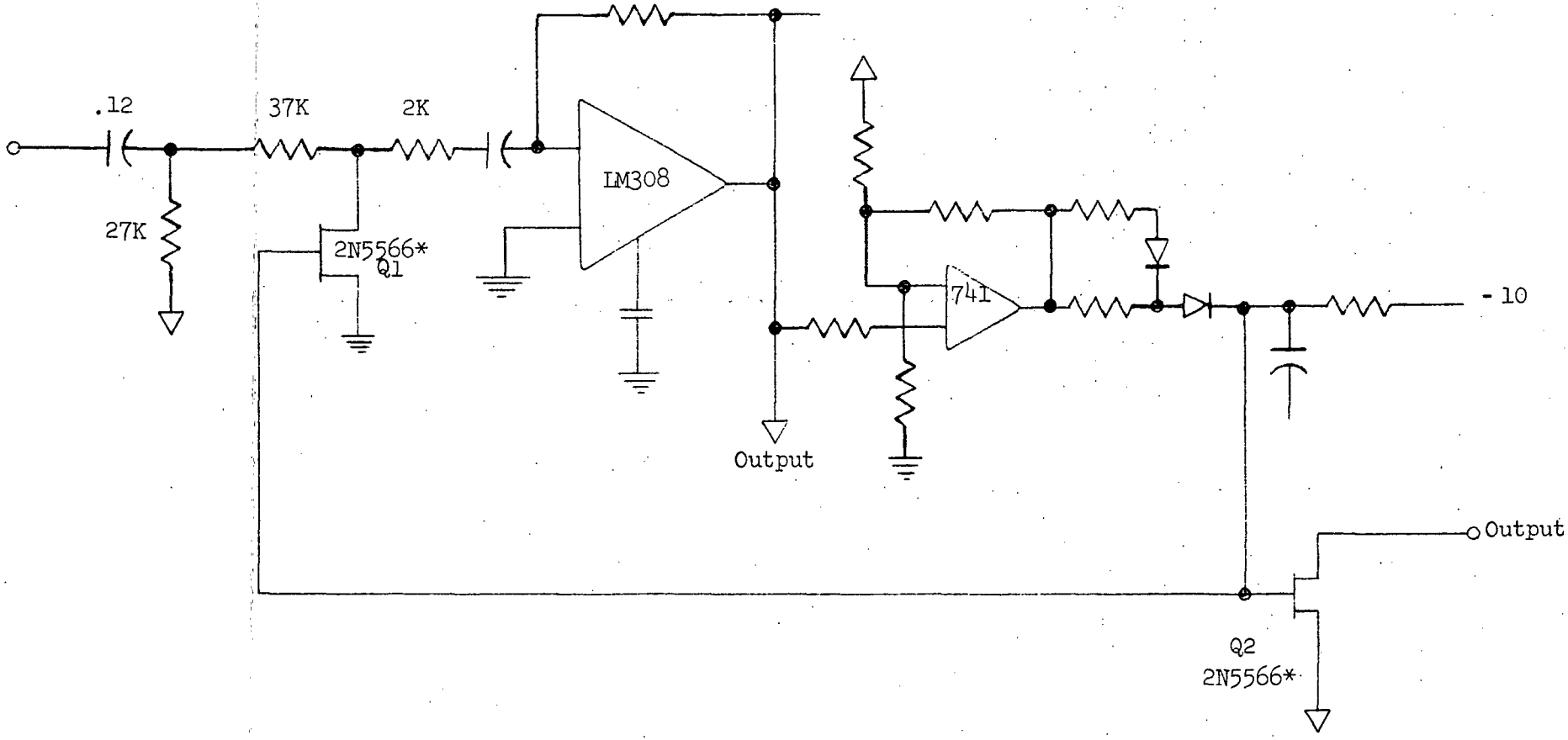
Let R_p $(R_e R_3)/(R_e + R_3)$

Then $A_{min} = 1 = \frac{R_p}{R_p + R_2} = \frac{R4}{R3}$

Therefore R_e 113

The R_{DS} (ON) for a 2N5566 is specified as 100 maximum and therefore provides the necessary R_e when fully turned on.

The fet acts as a variable resistance element as described above. The effective resistance of a fet in the triode or pre-pinch off region



* Matched Pair

FIGURE 3

is determined from the following expression for the drain current:

$$I_D = GV_{ds}\left(1 - \frac{V_{gs}}{VP} - Vds/2\right)$$

Re is therefore calculated as follows:

$$\frac{1}{R_e} = \frac{dId}{dVds} = G - G\,\frac{Vgs}{Vp} + G\,\frac{Vds}{Vp}$$

or

$$R_e = \frac{Vp}{G}\left(\frac{1}{Vp - Vgs + Vds}\right)$$

In this application it is necessary that R_e appear as a linear resistance to minimize distortion products. There were two methods which could have been used to accomplish this. If V_{DS} is superimposed on V_{gs}, the V_{DS} terms cancel in the expression for R_e. This would result in an extremely low distortion circuit. Unfortunately, the required coupling capacitor introduces additional time delay into the AGC loop which causes gain-control overshoot. The loop should ideally be controlled by a single time constant for optimum transient (attack) performance. The second method of achieving near linear performance is to limit the value of V_{DS} so that it is insignificant compared to V_p (about -3 volts for the selected fet) and V_{GS}. This approach has been incorporated into the UVP circuit. For sinusoidal signals, the p-p voltage across Q1 is limited to 6.3 mv. This results in (typically) less than 1% distortion for the AGC stage with R_e being given approximately as

$$R_e \quad 100\ (V_p/(V_p - V_{gs})$$

Note that this expression "blows up" as V_{gs} V_p as expected. It is

valid only for $V_{gs} \geq V_p$ and is taken as infinite for $V_{gs} < V_p$. The U1 stage provides a constant 25 db of gain when the normalized signal level falls below the voltage equivalent of -25 dbm or 123 mv p-p for a sinusoid. This gain is obtained when Q1 is pinched off so that fet variations do not affect this maximum gain or the input level at which it occurs. U2 (on substrate A1) is connected as a high gain noninverting amplifier with an offset provided by R_5. If the input to the stage is below the level determined by R_5 and R_7 ($10\ R_7/(R_5 + R_7) = 1.1$ volts), the output of U2 is saturated to approximately -9 volts. Under this condition C_4 will be discharged through R_{11} to about -10 volts, pinching off the gain control fet Q1. This results in the U1 stage exhibiting the maximum gain of 25 db. When the input to the U2 stage exceeds 1.1 volts, capacitor C4 is charged R_9 or R_{10} so that V_{gs} of Q1 is raised. As can be seen from the expression for R_e, this action reduces the value of R_e which reduces the stage gain. In this manner, the output of the U1 stage is maintained at the voltage equivalent of 0 dbm for all inputs (to the U1 stage) between -25 dbm and 0 dbm.

The initial attack time is governed by the R9 or C4 time constant. This results in a worst case attack time of less than 10msec. as required. For steady-state conditions and for small gain changes the gain control time constant is R_{10}, C_4, a much larger time constant. This results in reduced distortion, particularly at low frequencies.

The release time is governed by R_{11}, C_4 a time constant of 100 seconds. This results in a release time of approximately 10 seconds.

FET Q2 provides a method of externally determining AGC status. The gate

of Q2 (Q2 is half of a matched pair with Q1) is operated in parallel with that of Q1. The channel conductance of Q2 can, therefore, be monitored and serves as an indicator of AGC gain. The drain of Q2 (Pin 5) may be connected to the voltage divider R_{24} and R_{25} (Pin 3) to provide AGC status in the range of 0 to +5 volts.

II. Input Amplifiers

The input amplifiers (U1, U2 of substrate A2 and associated resistors) are designed to normalize the input signal levels to the voltage equivalent of -25 dbm to 0 dbm. This level is selected to optimize the signal-to-noise performance on the low-level input. To obtain these levels, the voltage gain of U1 (high level amplifier) is set at -25 db (1/17.8 volts/volt) and that of U2 (low level amplifier) at +30 db (31.6 volts/volt).

In the high level input amplifier, R_1 and R_4 provide a differential input impedance of 600 Ω as required. R_2, R_3, R_5 and R_6 are 1% resistors so that approximately 40 db of common mode rejection is obtained. The common mode voltage limit for the U1 amplifier stage is determined by the closed loop gain (1/17.8), the CMRR, and the common mode voltage limit of U1 at approximately 10KV! A more realistic limitation is imposed by the allowed power dissipation of R_1 and R_4. This restriction places the common mode limit @ 7 volts.

The low level amplifier, U2, is normally operated with a single-ended input with R_3 (Pin 31) grounded and signal applied to R_{11} (Pin 29). This results in > 150K Ω input impedance. A balanced 600 Ω input impedance can be achieved by the use of a 300 Ω resistor from Pin 31 to ground and a 320 Ω resistor from pin 29 to ground. The

voltage gain of the stage is 31.6 volts/volt with a CMMR of approximately 40 db. The output of U1 and U2 are available to use for the correct signal source to the AGC and VOX requirements.

III. Clipper

The clipper circuit is comprised of Q8, Q9, CR5, and associated components. The clip level reference is applied to the compensation input of U1 (LM308) and establishes peak clip levels within U1. If internal components are used pin 7 must be connected to pin 9. This will give reference clip levels of approximately $\pm$ 4.35V as the appropriate pins 6 and 9. This circuit clamps the output of the AGC Amp (U1) to 12 dbm $\pm$ 1 db at the AGC output (Pin 11). With an external resistor between pin 6 and pin 9, the AGC output can be clipped to levels between +15 dbm/and +3 dbm. By using separate reference resistors the clipping can be unbalanced for more efficient use of transmitter capability.

IV. VOX

The VOX circuitry of substrate A2 is comprised of amplifier U3 and circuitry associated with Q1 through Q3. The VOX input is taken from the normalized output of the U1 or U2 stage.

Amplifier U3 serves to increase the signal level so that precise amplitude detection can be performed. The smallest signal level which must activate the VOX is the voltage equivalent of -45 dbm (corresponding to -20 dbm on the high level input and -70 dbm on the low level input) or 02.3 mV p-p. If the free end of R15 is left open, the gain of the U3 stage is reduced to 2.44 so that a -25 dbm signal is required to activate the VOX.

This corresponds to 0 dbm on the high level input or -50 dbm on the low-level input. Intermediate levels can be programmed by placing the appropriate value resistor between the free end of R15 and ground.

The matched pair (Q1A-Q1B) serve as precise amplitude comparators. R20 and R21 set the slicing level at plus 150 mV. In this manner, Q1A will conduct only if the signal is above +150 mV. The comparator output drives Q2 to activate the R23, R24, C4 network.

The attack time is controlled by the R24 C4 time constant and is less than 5 msec. as required. The release time is governed by the R23 C4 time constant and is approximately 1 sec. after the input signal falls below the required activation level.

Q3 (substrate A1) serves to gate the output of the AGC into the filter section. Q3 (substrate A2), operated in parallel to Q3, substrate A1, provides an external indication of VOX status. The fet can be used to drive logic gates when connected to the junction of the R7 and R10 voltage divider providing output levels of 0-5 volt logic level on can be wire OR'd externally with other circuits.

V. Filter

Amplifiers U3 and U4 (substrate A1) and the associated passive components provide a bandpass filter. The two stages are identical with respect to their low pass characteristics. Each stage provides -40db/dec of rolloff for a total of -80db/dec. The 3db frequency of the filter at the high end is approximately 2.3 KHz.

At low frequencies, the gain of the U3 stage is controlled by the ratio

R13/R12. That of the U4 stage is controlled by the ratio R17/R16. The U4 stage appears as an inverting amplifier at low frequencies so that a high pass section is obtained by simply adding C7. The low frequency cutoff is then $1/2\pi$ R16 C7 or 96Hz.

VI. Output Buffer & Limiter

The output buffer provides current gain for driving a 600 Ω load. Transistors Q4 through Q7 (substrate A1) and associated resistors and diodes provide this function as well as providing over current protection for the output stage.

The necessary current gain is provided by Q6 and Q7 operating as a unity gain complimentary symmetry buffer. Diode Quad CR2 provides class AB biasing to eliminate crossover distortion. Resistors R22 and R23 prevent thermal runaway. The actual base drive for the output transistors comes from R20 and R21.

Output over current protection is provided by R22, R23, Q4, and Q5. If the output current exceeds approximately 30ma, Q4 and Q5 rob the output transistors of base drive. Note that 30ma of output current can only occur under a fault condition as ± 30ma into a 600 Ω load provides ± 18 volts of output swing capability.

VII. Power Conditioning

The input power supply levels are ±15 volts. These are dropped to ±10 volts by the use of zener diodes. High frequency noise is by-passed by C6 and C8. Reverse voltage protection is provided by CR1 and CR2.

UVP Performance Summary

A summary of the performance specifications follows.

Input Amplifiers

Voltage Gain of U1 stage:	-25db ± 1db
Voltage Gain of U2 stage:	+30db ± 1 db
CMRR (U1 stages):	> 40db at DC
	> 35db 0 to 2.3KHz
Input Impedance	U1 = 600Ω ± 10%
	U2 = ≥ 100K single ended
	600Ω balanced (ext component)
Output Impedance (both stages)	< 100Ω for output current < ± 5ma
Noise (both stages)	< the voltage equivalent of -65 dbm with inputs shorted to ground (300Hz to 2.3Khz)

AGC Circuit

Gain	The AGC shall maintain a constant level of 0 dbm ± .5db at the AGC output test pin for steady-state sinusoidal inputs between -25 dbm and 0 dbm. The AGC gain shall be a constant +25 dbm ± .25 db for inputs below -25 dbm. Inputs referred to above are measured at the AGC input pin (normalized inputs) and are to be between 300 and 2.3Khz.

Attack Time:

Attack time is measured using an 800Hz tone burst signal. The attack time needed to bring the AGC output down to 0dbm ±.5db following application of the tone burst (tone burst amplitude between -25dbm and 0dbm) shall not exceed 10msec. AGC gain prior to tone burst application shall be 25db.

Release Time:

AGC release time is to be measured using an 800Hz test tone. The test tone amplitude, following initial stabilization of the AGC with a 0dbm input, is to be abruptly reduced from 0dbm to -25dbm. The time required for the AGC output to return to 0dbm ±.5db shall be between 7 and 17 seconds.

Idle Gain:

For zero signal input, the AGC gain will idle at its maximum value of +25db. The AGC output is gated off under such conditions by the VOX circuitry and therefore appears to have zero gain at the UVP output.

Distortion:

The harmonic distortion produced by the AGC circuit shall be less than 1% for any normalized steady-state sinusoidal

input level between -25dbm and 0dbm at any frequency between 300Hz and 2.3Khz.

VOX Circuit

Filter: A single pole RC low pass filter is included in the VOX circuit to reduce noise sensitivity. The -3db frequency is 700 Hz ± 10%.

Threshold: The threshold is programmable between -45dbm and -25dbm (normalized inputs) when measured with a 300 Hz test tone. The VOX will operate at -25dbm ± 1db with no external resistors and at -45dbm ± 1db if the VOX gain pin is shorted to ground. Intermediate values are programmable with an external resistor connected between the VOX gain pin and ground.

Attack Time: The VOX attack time is measured as the time between application of a tone burst at 630 Hz and at a level 3db above the programmed threshold and the closing of the VOX switch as indicated at the VOX status pin. The attack time shall be less than 5 msec.

Release Time: The release time is to be measured with a 630Hz test tone. The release time

is the time required for the VOX switch to open, as indicated at the VOX status pin, following the time at which the test tone amplitude is reduced below the nominal VOX threshold level. This delay shall be 1 ± .2 sec.

Filter and Output Stage

3db (±1db) Bandwidth:	100Hz to 2.3 Khz
High Frequency Rolloff:	-80db/dec
Low Frequency Rolloff:	-20db/dec
Noise (with VOX off):	More than 60db below nominal (0dbm) output
Output Impedance:	$< 10\,\Omega$ at $\|Io\| < 20$ma

Clipper

Clip Level:	UVP is normally programmed to clip at 12dbm ± 1db at the AGC output. Clip levels between +15dbm and 3dbm can be programmed with an external resistor.

Input Power Requirements

Voltages	±15 volts, ±5%
Current	< 40ma

UVP PARTS LIST

Substrate No. A1

1. Resistors

	Value (OHMS)	Tol(%)*	Power**
R1	27 K		
R2	37 K	± 1	
R3	2 K		
R4	694 K	± 1	
R5	8.1K	± 1	
R6	1 K		
R7	1 K	± 1	
R8	68 K		
R9	5 K		
R10	430 K		
R11	100 MEG	± 10	
R12	38.7K	± 1	
R13	38.8K	± 1	
R14	19.4K		
R15	40 K		
R16	38.8K	± 1	
R17	38.8K	± 1	
R18	19.4K		
R19	60 K		
R20	10 K		
R21	10 K		
R22	20 Ω		

1. Resistors (continued)

	Value (OHMS)	Tol(%)*	Power**
R23	20 ~		
R24	20 K		
R25	20 K		
R26	10 K		
R27	10 K		
R28	10 K	± 1	
R29	15.4K	± 1	
R30	10 K	± 1	
R31	22 MEG		

* == ± 5% unless otherwise noted

** == ≤ 50 mw unless otherwise noted

2. Capacitors

	Value* (ufd)	Tol ± 5% (Except as Noted)
C1	.12	
C2	1	+ 80%, - 20%
C3	27 pfd	
C4	1	
C5	.006	
C6	.001	
C7	.1	
C8	.006	
C9	.001	
C10	.1	+80%, -20%
C11	.1	+80%, -20%
C12	.1	+70%, -20%
C13	.1	+80%, -20%

3. Amplifiers

U1 = LM 308, or equivalent

U2 = 741, or equivalent

U3 = 741, or equivalent

U4 = 741, or equivalent

4. FET'S

Q1 = 2N5566 } Matched Pair

Q2 = 2N5566 }

Q3 = 2N4393, or equivalent

5. Transistors

Q4 = 2N2222A

Q5 = 2N2907A

Q6 = 2N2222A

Q7 = 2N2907A

Q8 = 2N2222A

Q9 = 2N2907A

6. Diodes

CR1	1N914N - Dionics, or equivalent
CR2	DI914 - Quad, Dionics, or equivalent
CR3	DI914 - Quad, Dionics, or equivalent
CR4	DI914 - Quad, Dionics, or equivalent
CR5	DI914 - Quad, Dionics, or equivalent
CR6	1N914N - Dionics, or equivalent

UVP PARTS LIST

Substrate No. A2

1. Resistors

	Value (OHMS)	Tol(%)*	Power**
R1	300 ~		160 mw
R2	89 K	± 1	
R3	5 K	± 1	
R4	300 ~		160 mw
R5	84.3K	± 1	
R6	4.73K	± 1	
R8	5 K	± 1	
R9	158K	± 1	
R11	5 K	± 1	
R12	158K	± 1	
R13	9 K		
R14	200 K		
R15	10 K	± 1	
R16	157 K	± 1	
R17	246 K	± 1	
R18	20 K		
R19	100 K		
R20	1.31M	± 1	

1. Resistors (Continued)

	Value (OHMS)	Tol(%)*	Power**
R21	20 K	± 1	
R22	30 K		
R23	11 M		
R24	2 K		
R25	22 M		
R26	145 Ω		200 mw
R27	145 Ω		200 mw

*All Tol. ± 5% - except as noted

**Power ≤ 50 mw - except as noted

2. Capacitors

	Value (ufd)	Tol. ± 5% (Except as Noted)
C1	.1	
C2	.022	
C3	.1	
C4	.1	
C5	1	+ 80, - 20%
C6	.1	+80, -20%
C7	1	+ 80, - 20%
C8	.1	+80, -20%

3. Amplifiers

U1 = 741, or equivalent

U2 = 741, or equivalent

U3 = 741, or equivalent

4. Transistors

Q1 A,B = DI 4044, or equivalent

Q2 = 2N 2605A

5. FET'S

Q3 = 2N4393, or equivalent

6. Diodes

CR1 = Use C-B of 2N2222A

CR2 = Use C-B of 2N2222A

CR3 = Dickson CZA10D3, or equivalent

CR4 = Dickson CZA10D3, or equivalent

Applications of the UVP

The design of the UVP is an attempt to strike a balance between high flexibility and minimum external parts count.

There are four areas in the circuit where modifications are possible. These are:

I The low level input amplifier

II The clipping circuit

III The VOX amplifier

IV The signal gate (normally voice activated)

I. Low Level Input Amplifier

The low level input amplifier (U2 on substrate A2) provides up to 30 db of gain. The amplifier can be configured as a single-ended inverting, single-ended non-inverting, or differential input stage. The three configurations are illustrated in Figure 4.

Figure 4 (a) illustrates U2 used as an inverting, single-ended amplifier. The input impedance is $5K + R_X$. R_S is the source impedance associated with e_S. R_X is an externally added resistor which increases input impedance and decreases stage gain. The gain is given as $158K/(5K+R_X+R_S)$.

Figure 4 (b) illustrates U2 used a non-inverting, single-ended amplifier. The input impedance is $163K + R_X$ and the gain is:

$$A = (163K/5K)\ (158K/(163K + R_X + R_S))$$

Again, R_X is used to increase input impedance and decrease gain.

In the two single ended stages, a resistor between the input pin (pin 31 or 29) and ground can be used to reduce both input impedance and gain.

Capacitor coupling may be used for either of the two configurations.

If a balanced source is used to feed U2, the differential input configuration of Figure 4 (c) may be used. The differential input impedance is given by:

$$R_{in} = R_X \quad R_{p1} \quad 5K + R_X \quad R_{p2} \quad 163K$$

where signifies parallel resistance.

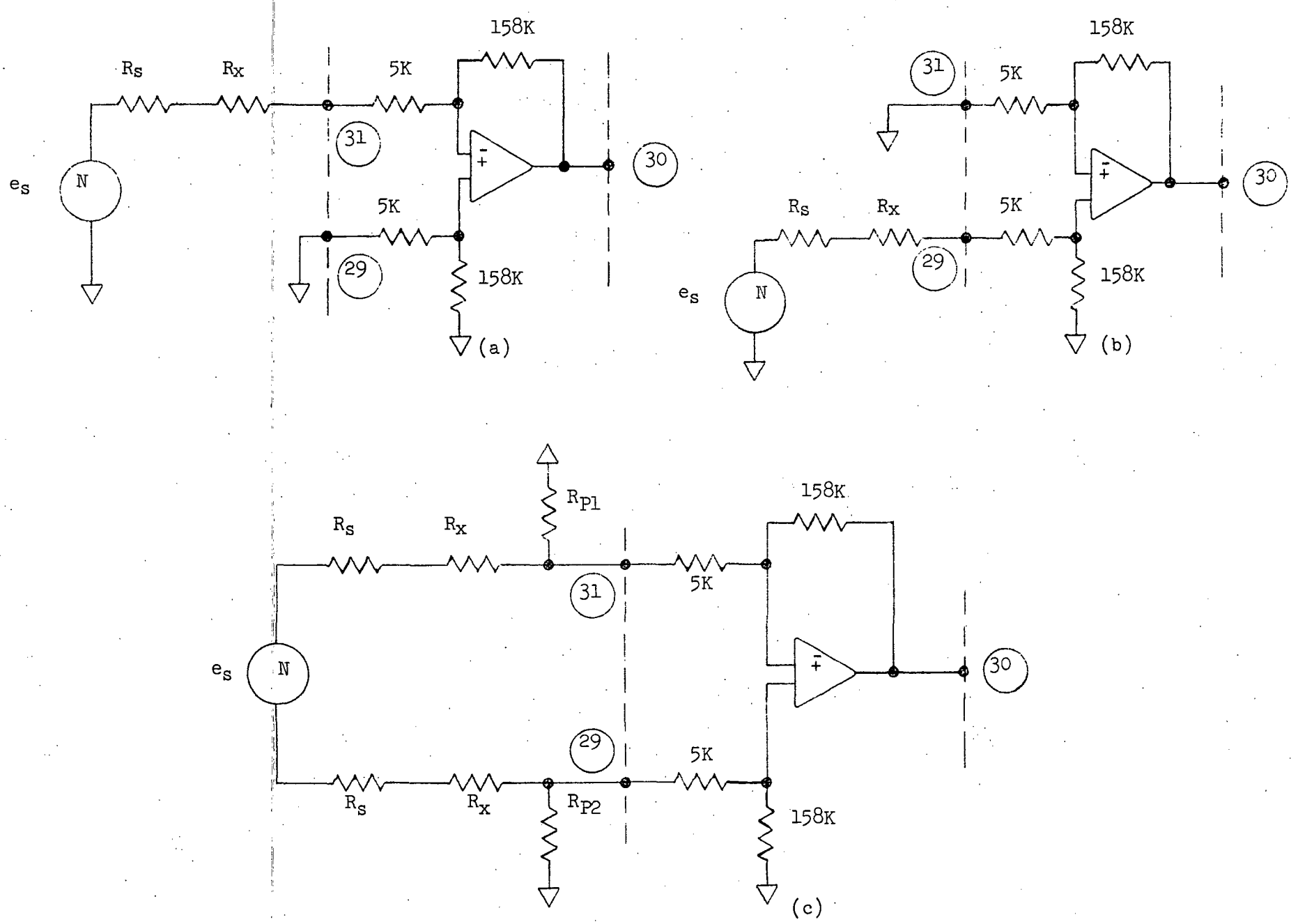

158K
Rs
Rx
5K
31
30
es
N
5K
29
158K
(a)
158K
31
5K
30
Rs
Rx
5K
es
N
29
158K
(b)
RP1
158K
Rs
Rx
31
5K
es
N
30
29
5K
Rs
Rx
RP2
158K
(c)

FIGURE 4

The expression for gain is cumbersome. From pins 31-29 the gain is 158K/5K. Appropriate correction must be made for the voltage dividers of R_{p1} with R_S and R_X as well as R_{p2} with R_S and R_X.

II. Clipping Circuit

The clipping level is determined by the voltage on pins 6 and 9. By connecting pins 7 and 9 externally, nominal clip levels of =10 + 20 (10K + 15.4K)/(10K + 15.4K + 10K) and +10 -20(10K + 15.4K)/(10K + 15.4K + 10K) volts are established. These levels, ±4.4 volts, correspond to a +12db in level out of the AGC amplifier, U1 (substrate A1).

A range of clip levels can be selected by using an external resistor. For clip levels above +12dbm, the following expression may be used:

$$e_c = \pm ((20(25.4K + R_X)/35.4K + R_X)) - 10)$$

where e_c is the resulting clip level and R_X is the value of an external resistor connected between pins 7 and 9. Clip levels between ±4.4 volts ($R_X = 0$) and approximately ±9 volts ($R_X \rightarrow \infty$) are programmable in this manner.

For clip levels below +12dbm, the following expression may be used:

$$e_c = \pm ((20(10K + R_X)/(20K + R_X)) - 10)$$

where e_c is the resulting clip level and R_X is the value of an external resistor connected between pins 6 and 9. Clip levels between approximately ±1 volt ($R_X \rightarrow 0$) and ±4.4 volts ($R_X = 15.4K$) are programmable in this manner.

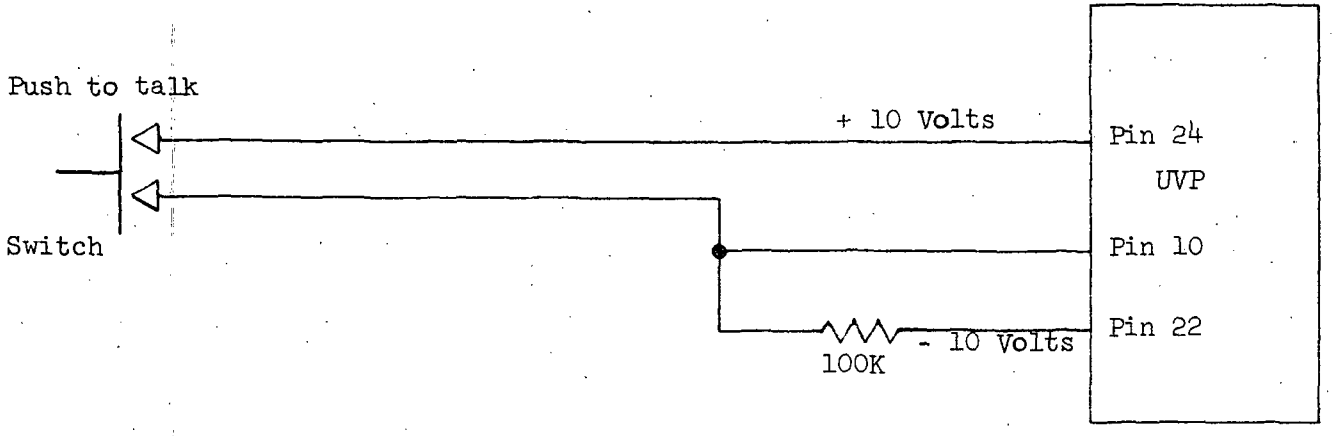
III. VOX Amplifier

The gain of the VOX amplifier may be changed to alter the input level at which the VOX will activate. This control is possible by using an external resistor between pin 29 and ground. With pin 39 open, the VOX gain is (246 + 10K + 157K)/(10K + 157K), resulting in a VOX activation level of '0' dbm at the high level input. With pin 39 shorted to ground, the gain is increased to (246K + 10K)/10K, resulting in a VOX activation level of -20dbm at the high level input. Intermediate values of VOX gain can be programmed with an external resistor between pin 39 and ground.

IV. Signal Gate

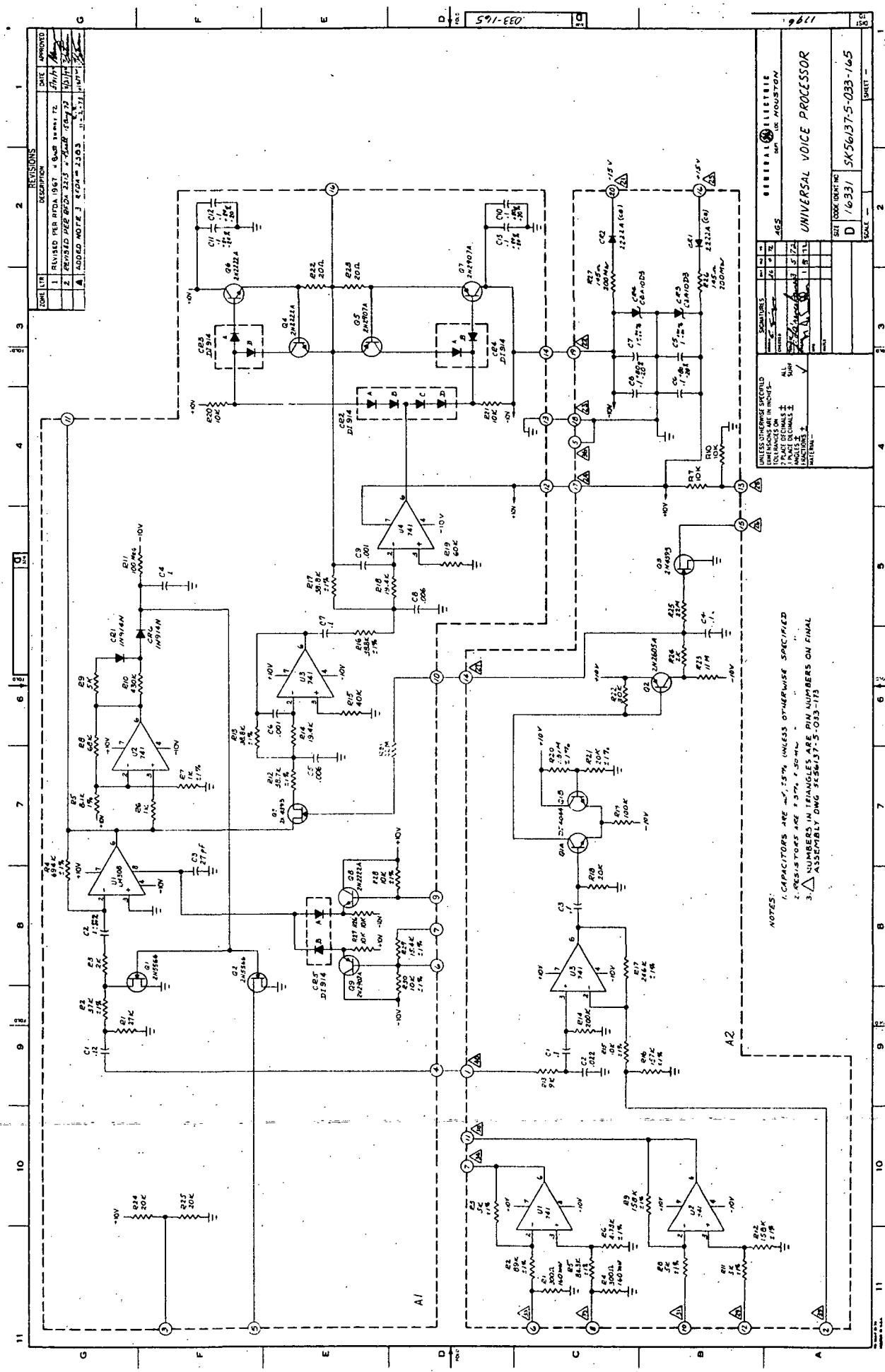
The signal gate Q3 on substrate A1 is normally controlled by the VOX circuitry on substrate A2. The gate will be off (no output) when the voltage at pin 10 is negative (typically -10 volts) and on (signal gated through the filters and output stage) when the voltage at pin 10 is positive (typically +10 volts).

If 'push-to-talk' operation is desired in place of VOX operation, the external connection between pins 10 and 27 must be broken. The push-to-talk switch can then be wired to pin 10 to provide the necessary control levels. A suggested arrangement is shown in Figure 5.



PUSH-TO-TALK OPERATION

FIGURE 5


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
1 REVISED PER RFDA 1967 5/11/71
2 REVISED PER RFDA 2218 10/13/71
4 ADDED NOTE 3 11-5-71
UNIVERSAL VOICE PROCESSOR
SIZE D CODE IDENT NO 16331 SX561375-033-165
SCALE — SHEET —
NOTES:
1. CAPACITORS ARE +/-5% UNLESS OTHERWISE SPECIFIED
2. RESISTORS ARE ±1% ¼W
3. NUMBERS IN TRIANGLES ARE PIN NUMBERS ON FINAL ASSEMBLY DWG SX561375-033-113
A1
A2

UVP - EXTENSIONS AND POSSIBLE NEW AREAS OF INVESTIGATION

The UVP Program has demonstrated the usefulness of the hybrid approach for a moderately complex circuit realization. The hybrid technology continuously advances, making available new opportunities for improvement in systems such as the UVP. Two general areas which could benefit the UVP as of this writing are (1) the refinement of the UVP as a voice processor and (2) the extension of the old capabilities of the UVP.

Specific proposals in the two general areas are:

1. Refinement of UVP

   (a) Reduce the complexity by reducing the numbers of options available. If the specific input levels and clip levels could be established, for example, considerable circuit simplification would result.

   (b) Develop a power supply which operates directly from the spacecraft +28 volt bus. New three terminal IC regulators appear very attractive for this application.

   (c) Investigate new methods of filtering to reduce the component count in the band pass filter circuitry.

   (d) Replace the presently discrete design output stage with an IC. Such an IC would incorporate CR2a, b, c, d; CR3a, b; CR4a, b; R20, R21, R22, R23; Q4, Q5, Q6, and Q7 from substrate A1. The IC would also have application as a current limited power buffer for operational amplifiers.

   (e) Reduce substrate count to one by virtue of (a), (c), and (d), above.

2. Extension of Capabilities

   Provide an earphone amplifier on the substrate for the "uplink" communication. The IC mentioned in (d), above, could be used here.

UNIVERSAL VOICE PROCESSOR DEVELOPMENT

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